ACCESS CIRCUIT AND METHOD FOR ALLOWING EXTERNAL TEST VOLTAGE TO BE APPLIED TO ISOLATED WELLS

ABSTRACT OF THE DISCLOSURE

An access circuit selectively couples an externally accessible terminal to each of a plurality of isolated DRAM wells in which respective DRAM arrays are fabricated. The access circuit for each well includes first and second transistors fabricated in respective wells coupled between the externally accessible terminal and a respective one of the DRAM wells. The well of the first transistor is coupled to the externally accessible terminal, and the well of the other transistor is coupled to a respective DRAM well. A control circuit applies select signals to gate electrodes of the first and second transistors. The control circuit includes respective shunt transistors that shunt the gate electrodes to the source regions of the first and second transistors when the transistors are turned off to isolate the respective DRAM wells from the external terminal regardless of the magnitude and polarity of a test voltage applied to the externally accessible terminal.